Rockchip RM182XMC0 Datasheet

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Revision History

Date	Revision	Description
2026-02-05	1.0	Initial Release
2026-04-05	1.1	• Change PCIe M.2 KEY M to PCIe M.2 KEY B-M • PIN34, PIN36 compatible USB_D+ & USB_D- • Change PCIe2.1 Interface to Multi-PHY Interface in Chapter 1.2.7
2026-06-17	1.2	• Revise section 2.3,add section 2.3.2 RM182XMC0_V22 • Upadate Table 2 1 RM182XMC0 Pin Number Order Information

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Chapter 1 Introduction

1.1 Overview

RM182XMC0 (corresponding product name: RM1820MC0 or RM1828MC0) is based on the RK182X, the high-performance AI co-processor SoC (RK182X includes RK1820 and RK1828, RK1820 support 3B large model, RK1828 support 7B large model), is designed for machine learning application, especially for Large Language Model (LLM) and Vision Language Model (VLM) related application.

RK182X is based on three 64-bit independent RISC-V cores with FPU. There is a 32KB I-cache,32KB D-cache and 128KB L2 cache for each core.

The built-in NPU Support INT4/INT8/INT16/FP8/FP16/BF16 hybrid operation and computing power is up to 20TOPS. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK182X has an extreme high bandwidth built-in DRAM.

1.2 Features

1.2.1 RK182X Co-Processor

- Three RISC-V cores abbreviated as SRV, VRV0 and VRV1
- SRV is implemented with RV64GCB ISA and VR0/VRV1 is implemented with RV64GCBV ISA
- All cores are integrated FPU with RISC-V H/F/D precision
- Each core has 32KB L1 I-Cache, 32KB L1 D-Cache and 128KB L2 cache
- VRV0 and VRV1 is integrated with 128-bit vector unit

1.2.2 RK182X Memory Organization

- RK182X Internal on-chip memory
  - Bootrom
    - Support system code download by the following interface:
      - PCIe2.1 interface
      - USB3.0 interface
  - 512KB system SRAM
  - Built-in Dynamic Memory Interface
    - RK1820 Density is 2.5GB
    - RK1828 Density is 5GB

- RM182XMC0 External off-chip memory
  - Combo SDMMC Interface, work at the following mode
    - eMMC (option)
      - Fully compliant with JEDEC eMMC 4.51 specification
      - Support HS200, but not support CMD Queue
      - Support three data bus width mode: 1bit, 4bits and 8bits

1.2.3 RK182X System Component

- CRU (clock & reset unit)
  - Support total 4 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU (power management unit)

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- Multiple configurable work modes to save power by different frequency or automatic clock gating control
- Support 3 separate voltage domains
- VDD_TOP, VDD_LOGIC, VDD_PMU

- Timer
  - Support 6 timers with 64bits counter and interrupt-based operation
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Three Watchdogs

- Interrupt Controller
  - Support 160 interrupt sources input from different components inside SoC for SRV and 64 interrupt sources input for VRV
  - Support 1 software-triggered interrupt in m-mode and s-mode each
  - Input interrupt level is fixed, high-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Support 2 physical channels
  - Support 22 groups of peripheral request interfaces
  - Support 24 logic channels, each logic channel support the following feature
    - Support the data transfer of memory-to-memory, memory-to-peripherals, peripherals-to-memory
    - Support Linked list DMA function to complete scatter-gather transfer
    - Support three kinds of multi-block transfer: contiguous address, auto reload, link list

- Secure System
  - Support one cipher engine
    - Support Symmetrical algorithms
      - AES-128, AES-192, AES-256, SM4
      - ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode for AES and SM4
    - Hash algorithm
      - SHA-1, SHA-256/224, MD5, SM3 with hardware padding
      - HMAC of SHA-1, SHA-256, MD5, SM3 with hardware padding
    - Asymmetrical algorithms
      - RSA (up to 4096 bits), ECC (up to 256 bits), SM2
    - Key-ladder (KL)
      - Support obtaining the root key from OTP or RKRNG and deriving it
      - Support writes out root key or derived key to some specific modules
      - Number of stages can be configured

- Mailbox
  - Twelve mailboxes in SoC used to service different RISC-V communication

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1.2.4 RK182X JPEG CODEC

- JPEG encoder
  - Supports Baseline (DCT sequential)
  - Supports JPEG file interchange format (JFIF) 1.02
  - Supports image size is from 16x16 to 65520x65520
  - Supports YUV400/YUV420/YUV422/YUV444

- JPEG Decoder
  - Support Baseline (DCT sequential)
  - Support JPEG file interchange format (JFIF) 1.02
  - Support image size is from 48x48 to 65520x65520
  - Support YUV400/YUV420/YUV422/YUV440/YUV411/YUV444/RG888/RGB565

1.2.5 RK182X Neural Process Unit

- Rockchip NPU engine:
  - Up to 20 TOPS for INT8
  - Support INT4/INT8/INT16/FP8/FP16/BF16 operation
  - Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

1.2.6 RK182X 2D Graphics Engine

- 2D Graphics Engine (RGA)
- Data format
  - SRC0 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551
    - RGB888P/RGB565
    - YUV422-P/YUV422-SP-8bit/10bit (clip to 8bit after input)
    - YUV420-P/YUV420-SP-8bit/10bit (clip to 8bit after input)
    - YUV444I/YUV444SP-8bit
    - YVYU422-8bit
    - YUV400-8bit
    - TILE4X4 YUV420/422/444-8bit
    - TILE4X4 YUV420/422/444-10bit (clip to 8bit after input)
    - BPP1/2/4/8
  - SRC1 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
    - RGB888P/RGB565
  - Output data format (all YUV format is 8bit):
    - ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
    - RGB888/RGB565
    - YUV420/YUV422 P/SP
    - YUV400/Y4
    - YUV444SP/444I
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution : 8192x8192 source, 4096x4096 destination
- Scaling
  - Down-scaling: Average/Bilinear filter
  - Up-scaling: Bi-cubic filter(source>1992 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
  - 0, 90, 180, 270-degree rotation
  - x-mirror, y-mirror operation
  - Mirroring and rotation co-operation
- BitBLT
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)

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- Two source BitBLT
- A+B=B only BitBLT, A support rotate & scale when B fixed
- A+B=C second source (B) has same attribute with (C) plus rotation function

- Alpha Blending
  - Comprehensive per-pixel alpha (color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y) +SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- OSD Automatic Inversion
  - Support OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
  - Support SRC0 and OSD overlay

1.2.7 RM182XMC0 Connectivity interface

- Multi-PHY Interface
  - Support one PCIe2.1 controller and one USB3.0 DRD controller (multiplex to one of the PHY)
  - Support one of the following interfaces for each multi-PHY
    - USB3.0 DRD
    - PCIe2.1
  - USB 3.0 Dual-Role Device (DRD) Controller
    - Static USB3.0 Device
    - Static USB3.0 xHCI host
  - PCIe2.1 interface
    - Compatible with PCI Express Base Specification Revision 2.1
    - Support one lane
    - Support dual operation mode:Root Complex (RC) and End Point (EP)
    - Support 2.5Gbps and 5.0Gbps serial data transmission rate per lane per direction

- USB 2.0 DRD (Dual-Role Device)
  - Support one USB2.0 DRD (Dual-Role Device)
  - Compatible with USB 2.0 specification
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

1.2.8 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (a weak pull-up and a weak pull-down)
  - Support configurable drive strength

- OTP
  - Support 8K bits size, 6.5K bits for secure application
  - Support Program/Read/Idle mode

1.3 RM182XMC0 Diagram

The following figure shows the basic block diagram.

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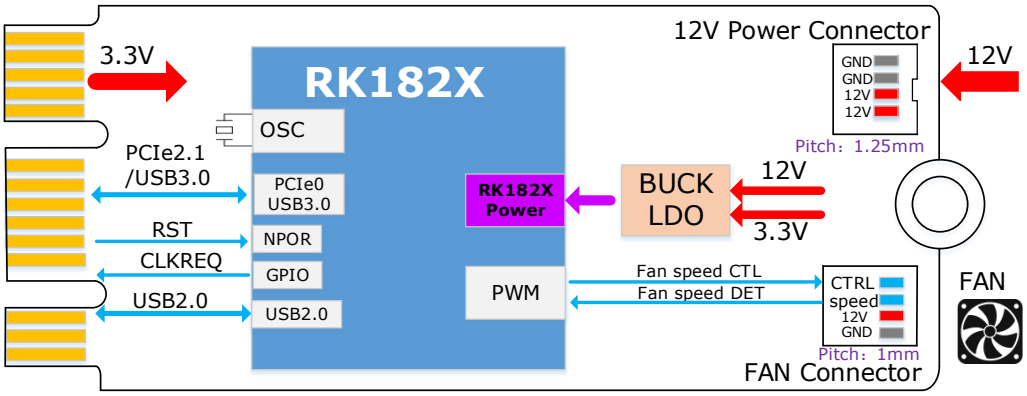

Fig. 1-1 RM182XMC0 Block Diagram

1.4 RM182XMC0 Typical Application

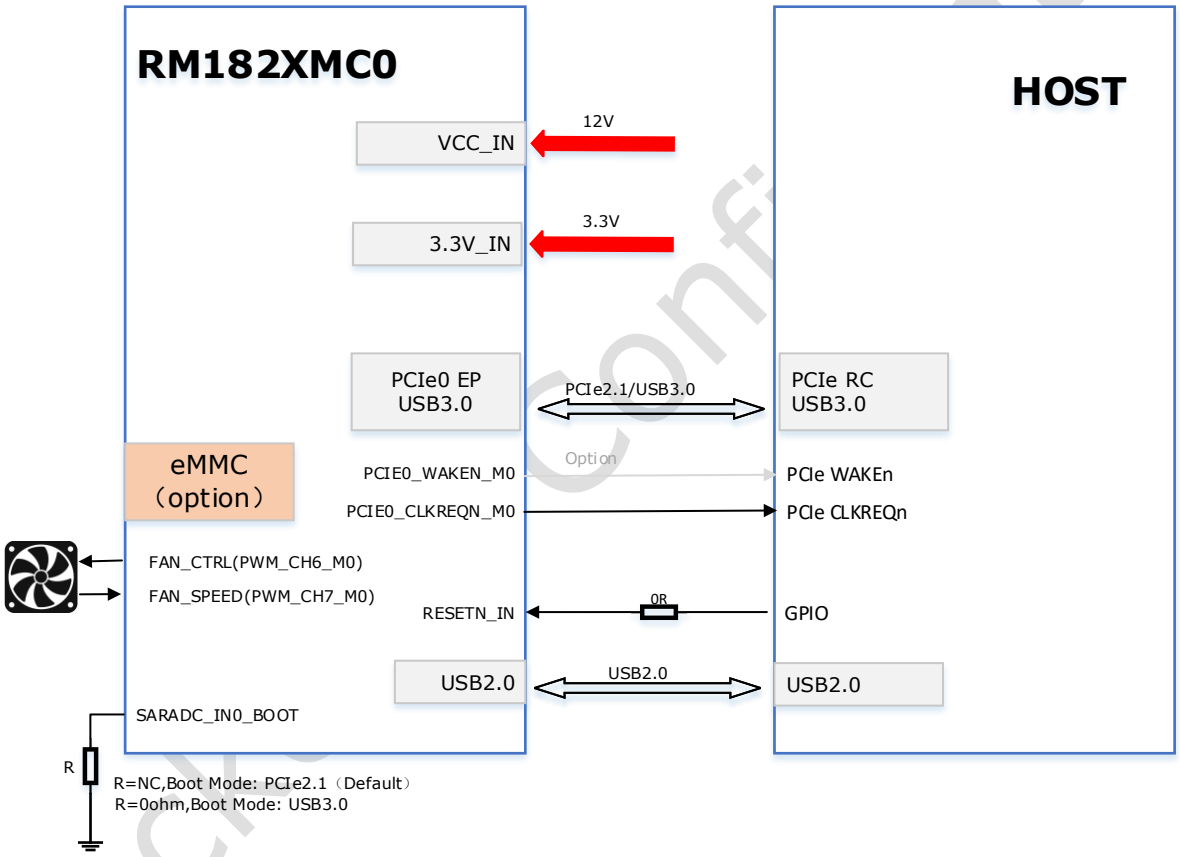

Fig. 1-2 RM182XMC0 Typical Application Block Diagram

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Chapter 2 Module Information

2.1 Module Size

- 22mm x 80mm x6mm (RM182XMC0)
- 25mm x 81mm x23.05mm (RM182XMC0-F)

2.2 External Connector

- The Module exposes a M.2 Key B-M connector.

2.3 Module Dimension

Note: All dimensions given in millimeter units.

2.3.1 RM182XMC0_V20

The following figure shows the RM182XMC0_V20 version

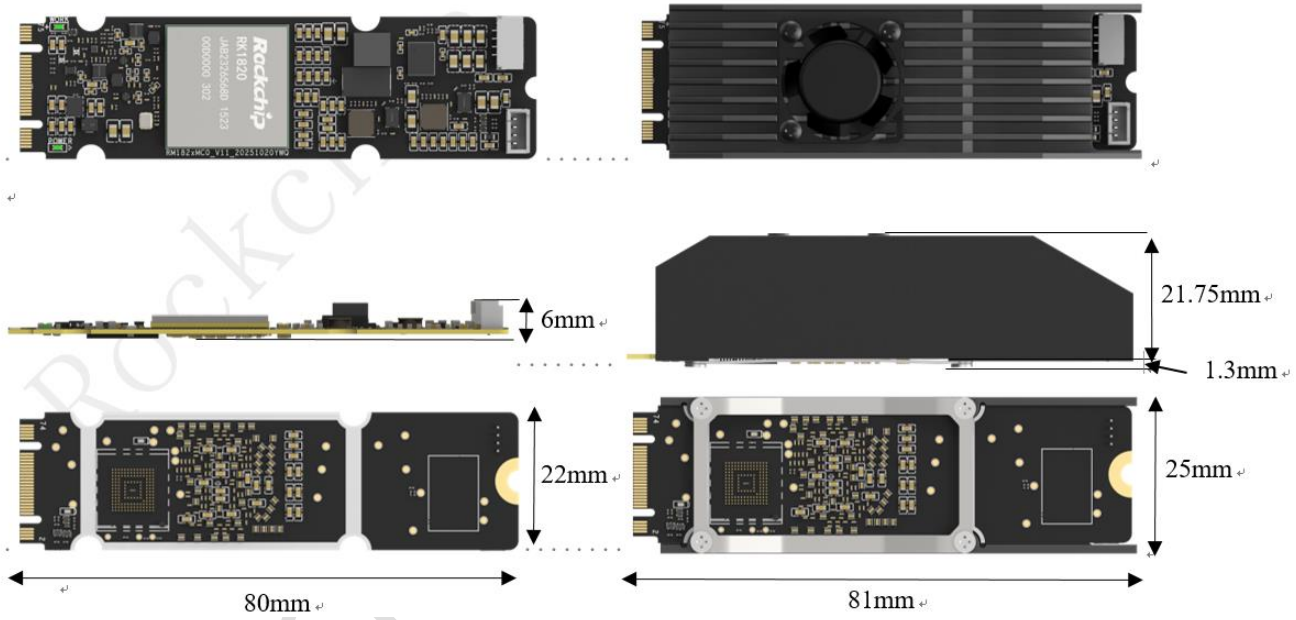

Fig. 2-1 RM182XMC0_V20 View (include without fan and with fan)

2.3.2 RM182XMC0_V22

The following figure shows the RM182XMC0_V22 version

Note: Compared with RM182XMC0_V20, the main modification is: Structural Change of Heat Dissection Metal Part, This is a minor change, only changing the fixing screw of M.2 lock attachment，This version is compatible with existing hardware and software designs
Detailed descriptionPlease refer to《Rockchip RM182XMC0&RM182XMC0-F产品变更-RKPCNMI20051-20260617.pdf》

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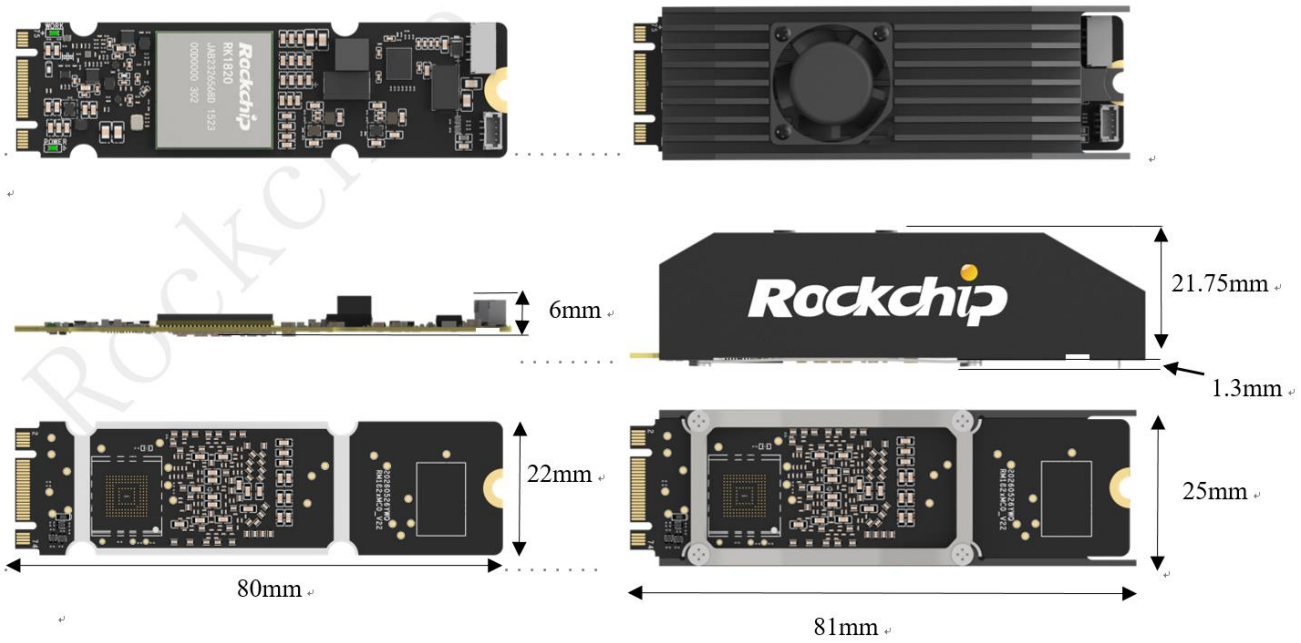

Fig. 2-2 RM182XMC0_V22 View (include without fan and with fan)

2.4 Module Connector Pin Number List

Table 2 1 RM182XMC0 Pin Number Order Information

Pin Name	Pin #		Pin #	Pin Name
CONFIG_3=GND	1		2	3.3V
GND	3		4	3.3V
NC	5		6	NC
NC	7		8	PLN#(I)(0/1.8/3.3V)
NC	9		10	LED_1#(O)(OD)
NC	11		20	NC
CONFIG_0=GND	21		22	NC
NC	23		24	NC
NC	25		26	NC
GND	27		28	PLA_S2#(O)(0/1.8V)
PETn1	29		30	NC
PETp1	31		32	GND
GND	33		34	USB_D+
PERn1	35		36	USB_D-
PERp1	37		38	GND
GND	39		40	SMB_CLK(I/O)(0/3.3V)
PETn0/USB0_DRD_SSTXN_M0	41		42	SMB_DATA(I/O)(0/3.3V)
PETp0/USB0_DRD_SSTXP_M0	43		44	ALERT#(O)(0/3.3V)
GND	45		46	NC
PERn0/USB0_DRD_SSRXN_M0	47		48	NC
PERp0/USB0_DRD_SSRXP_M0	49		50	PERST#(I)(0/1.8/3.3V)
GND	51		52	CLKREQ #(I)(0/3.3V)
REFCLKN	53		54	PEWake#(IO)(0/3.3V)
REFCLKP	55		56	Reserved for MFG Data
GND	57		58	Reserved for MFG Clock
NC	67		68	SUSCLK(I)(0/1.8/3.3V)
CONFIG_1=NC	69		70	3.3V
GND	71		72	3.3V
VIO_CFG(O)	73		74	3.3V
CONFIG_2=GND	75			

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2.5 Pin Function description

See the RM182XMC0 Pinout for details on connecting to each of the interfaces.

Table 2-1 Power and System Control Pin Descriptions

Pin#	Signal Name	Description	Direction	Pin Type
2 4 70 72 74	3.3V	Main power: Supply provides power to the module.	Input	3.3V
50	PERST#(I)(0/1.8/3.3V)	Module Reset. Reset to the module when driven low by HOST.	Input	1.8V/3.3V Domain
56	SARADC_IN0_BOOT	BOOT mode configuration. 10kΩ pull-up to 1.8V , 2.7kΩ pull-up to GND ,on the module.	Input	Input

Table 2-3 VCC_IN Power Pin Descriptions

Pin#	Signal Name	Description	Direction	Pin Type
1 2	VCC_IN	Main power: Supply provides power to the module.	Input	8V to 14.4V
3 4	GND			

Table 2-4 PCIe/USB Pin Descriptions

Pin#	Signal Name	Description	Direction	Pin Type
43	PETp0/USB0_DRD_SS TXP_M0	PCIe transmit differential Positive USB0 DRD SuperSpeed transmit differential Positive(Mux0)	Output	Combo PHY
41	PETn0/USB0_DRD_SS TXN_M0	PCIe transmit differential Negative USB0 DRD SuperSpeed transmit differential Negative(Mux0)	Output	Combo PHY
49	PERp0/USB0_DRD_SS RXP_M0	PCIe receive differential Positive USB0 DRD SuperSpeed receive differential Positive(Mux0)	Input	Combo PHY
47	PERn0/USB0_DRD_SS RXN_M0	PCIe receive differential Negative USB0 DRD SuperSpeed receive differential Negative(Mux0)	Input	Combo PHY
55	REFCLKP	PCIe differential clock Positive,Support input or output	Bidir	Combo PHY
53	REFCLKN	PCIe differential clock Negative,Support input or output	Bidir	Combo PHY
34	USB_D+	USB0 DRD HS/FS/LS Data Plus	Bidir	USB PHY
36	USB_D-	USB0 DRD HS/FS/LS Data Minus	Bidir	USB PHY

Table 2-5 GPIO Power Domain Descriptions

Pin#	Signal Name	Description	Direction	Pin Type
50	PERSTN	PCIe Global reset	Input	1.8V/3.3V
52	CLKREQN	PCIe reference clock request	Output	3.3V

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Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute Ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for VCC_IN	VCC_IN	-0.3	18	V
Supply voltage for 3.3V	3.3V	-0.3	3.8	V
Max Conjunction Temperature	Tj	NA	105	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended Operating Condition

Parameters	Related Power Group	Min	Typ	Max	Unit	Note
Supply voltage for VCC_IN	VCC_IN	8.0	12.0	14.4	V	1
Supply current for VCC_IN	I_{VCC_IN}	2.0	-	4.0	A	
Supply current for 3.3V	3.3V	2.97	3.3	3.63	V	
Storage Temperature	Tstg	-20	-	70	℃	
Storage relative humidity		30	-	70	%	3
Ambient Operating Temperature	Ta	-10	25	55	℃	4
Max Conjunction Temperature	Tj	-	-	95	℃	

Notes:
1. Considering the maximum contact current rating of each contact of M.2 Socket (generally 0.5A), it is recommended that the power supply voltage is 12V. When the power supply capacity can provide more than 40W, each pin should not exceed 0.5A.
The power consumption corresponding to different performance modes，see RM182XMC0 Thermal Design Guide for details.
2. By default, it is only used for VCCIO2/VCCIO3 power domain.If external devices also want to use it, the VCC_IN input power should be increased accordingly.
3. No condensation
4. Customers should consider specific thermal design for the final product based on the specific environment, performance requirements and operational conditions.

3.3 DC Characteristics for GPIO

Table 3-3 DC Characteristics for GPIO

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VCCIO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VCCIO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VCCIO	V
	Input High Voltage	Vih	0.65*VCCIO	NA	VCCIO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VCCIO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm

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3.4 Electrical Characteristics for Multi -PHY

Table 3-4 Electrical Characteristics for PCIe PHY

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Transmitter						
Differential p-pTx voltage swing	$V_{TX-DIFF-PP}$		0.8	NA	1.2	V
Low power differential p-p Tx voltage swing	$V_{TX-DIFF-PP-LOW}$		0.4	NA	1.2	V
Tx de-emphasis level ratio	$R_{TX-DIFF-DC}$		80	NA	120	ohm
Single Ended Output Resistance Matching	$R_{TX-DC-OFFSET}$		NA	NA	5	%
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		NA	NA	600	mV
Output rising time for 20% to 80%	Tr		25	NA	NA	ps
Output falling time for 20% to 80%	Tf		25	NA	NA	ps
AC Coupling Capacitor(USB3.0/PCIE)	C_{TX}		75	NA	200	nF
Unit Interval	UI		399.88	NA	400.12	ps
Input Voltage Swing	$V_{rxdpp-c}$		250	NA	1200	mV
Input differential impedance	R_{rxd-c}		80	NA	120	ohm
Single Ended input Resistance Matching	$T_{rxd-c-ms}$		NA	NA	5	%

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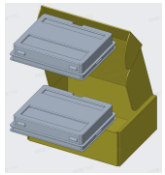
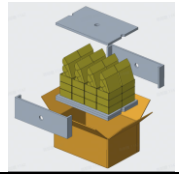
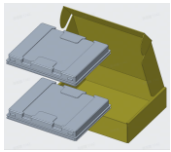
Chapter 4 Order Information

Product Model	Description	HS Code	RoHS Status	MSL	Package Quantity	Unit Net Weight (g)
RM1820MC0	RM1820MC0 Module without Fan	8473309000	RoHS	MSL3	Unit per anti-static tray: 10 pcs  Unit per inner box: 2 trays, 20 pcs  Unit per box: 24 inner boxes, 480 pcs 	10.6
RM1828MC0	RM1828MC0 Module without Fan		RoHS	MSL3		10.6
RM1820MC0-F	RM1820MC0 Module with Fan		RoHS	MSL3	Unit per anti-static tray: 10 pcs  Unit per inner box: 2 tray, 20 pcs  Unit per box: 12 inner boxes, 240 pcs	53.1
RM1828MC0-F	RM1828MC0 Module with Fan		RoHS	MSL3		53.1

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					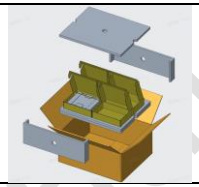		

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